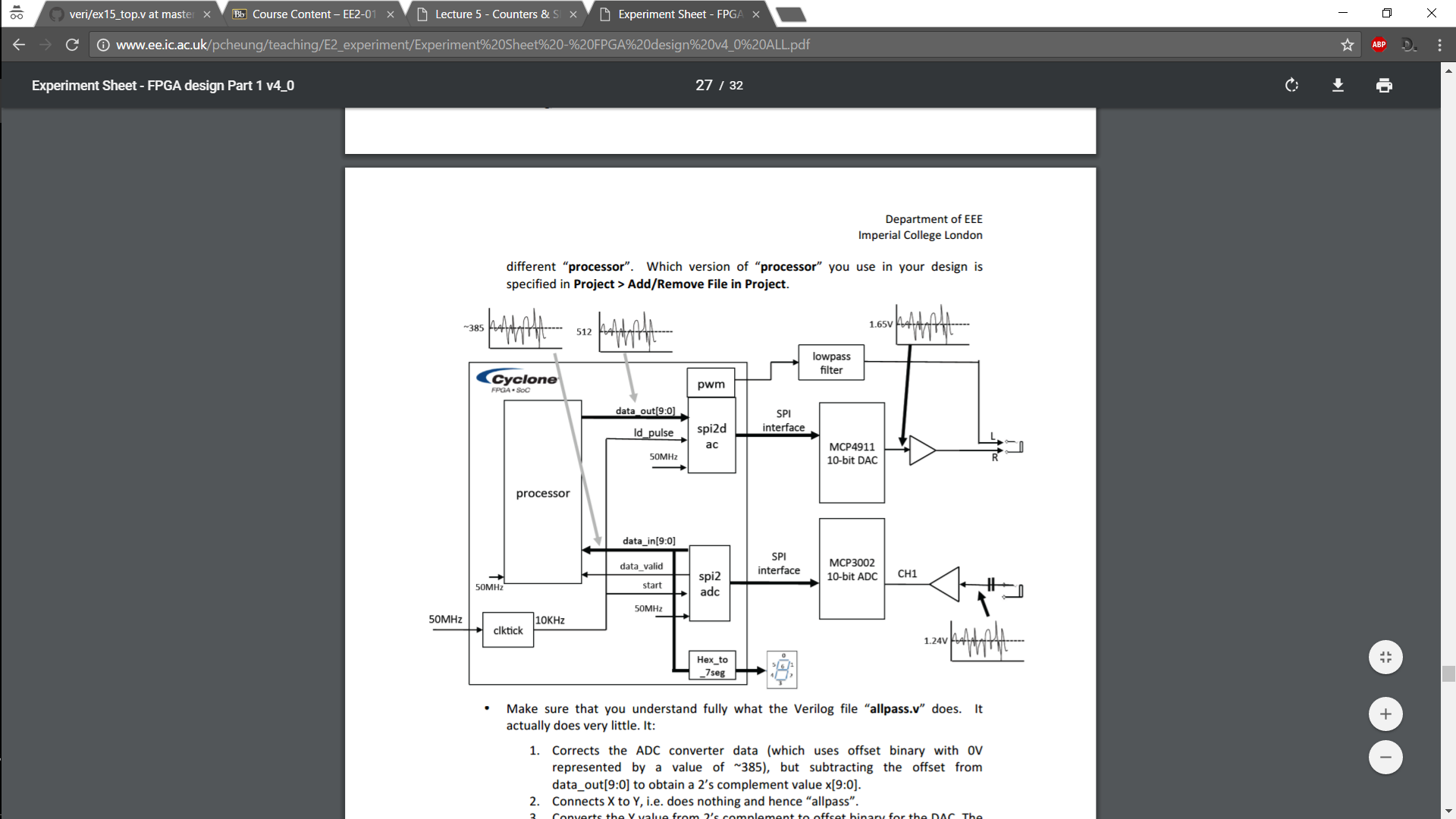
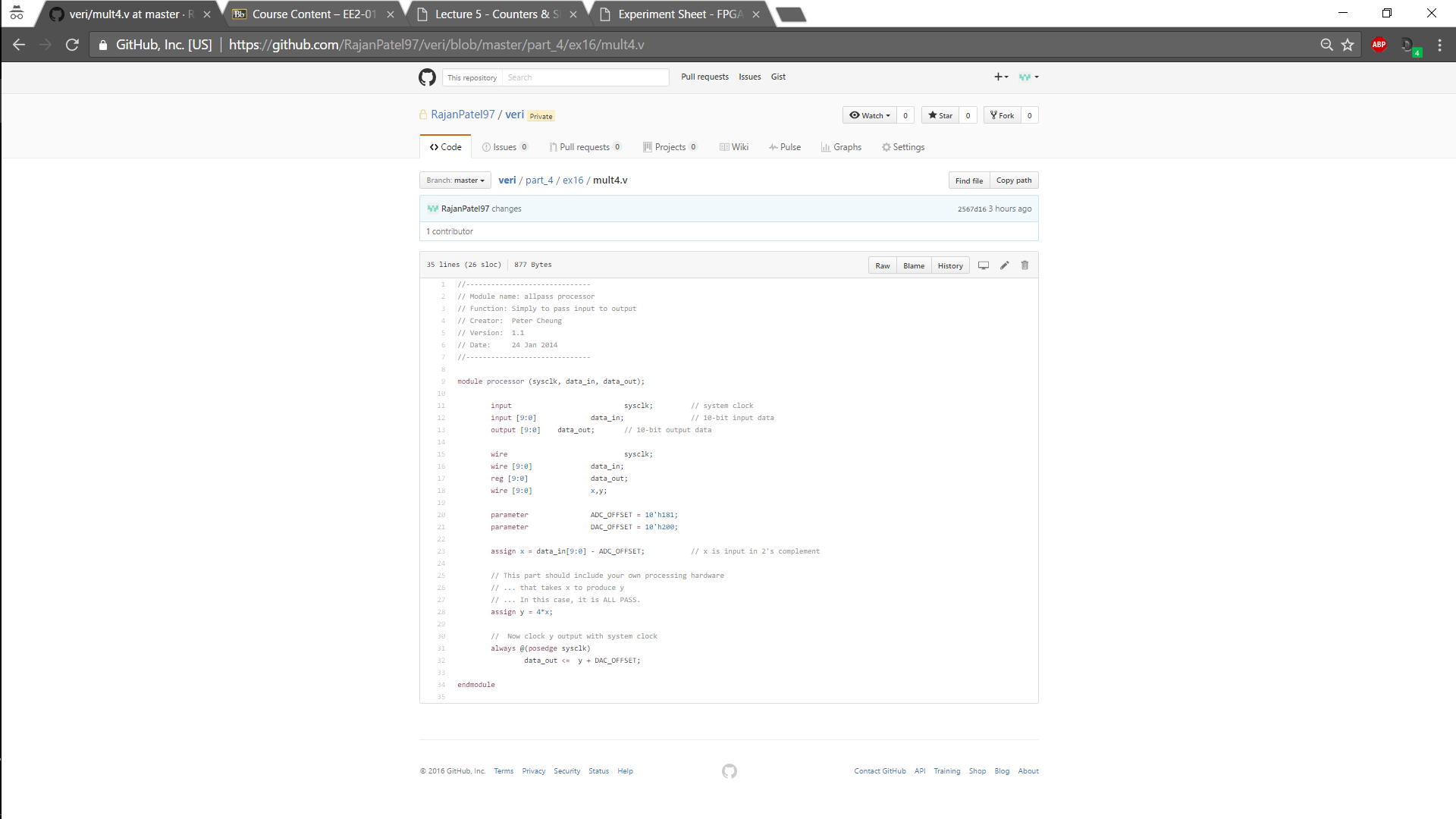
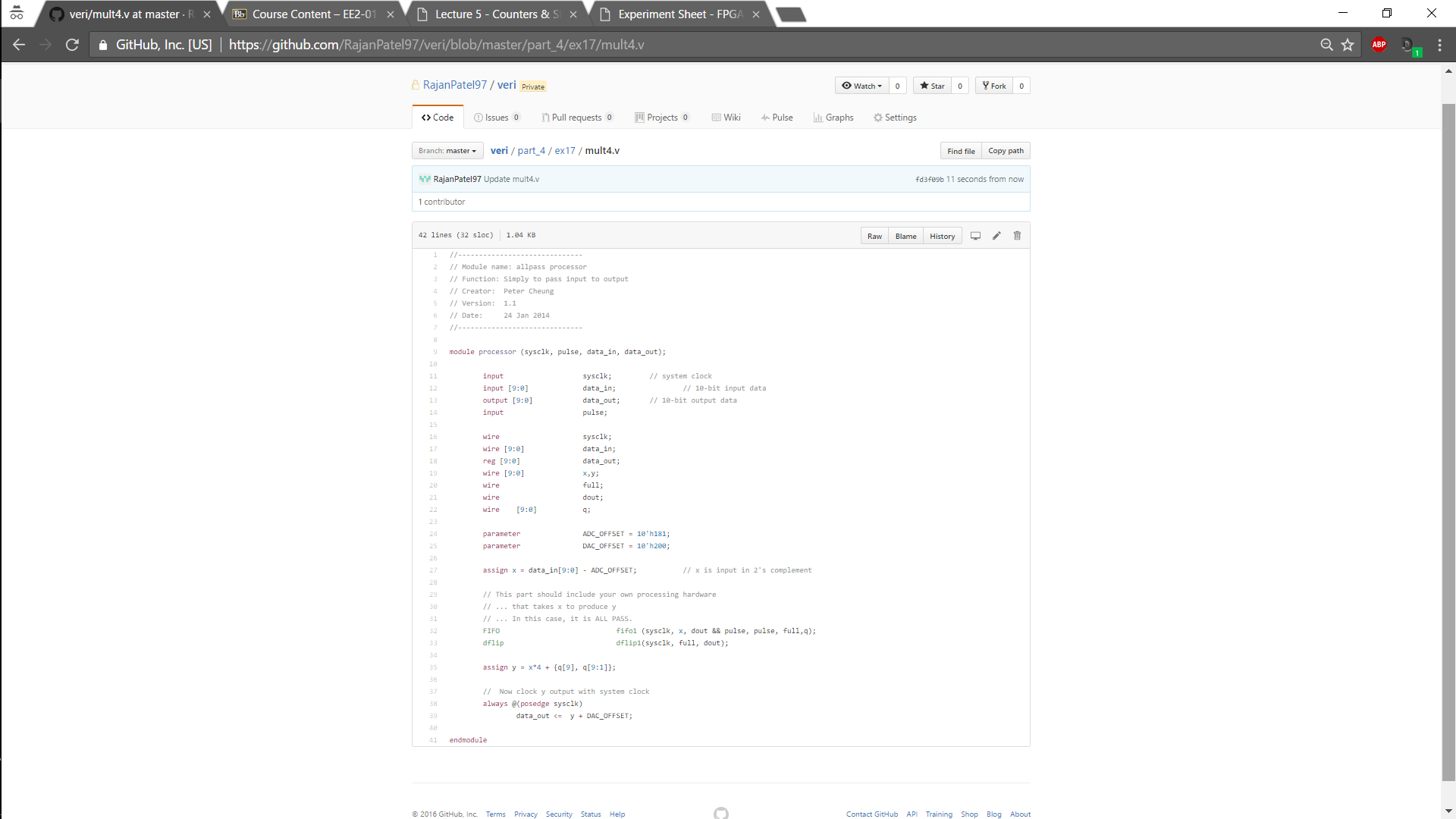
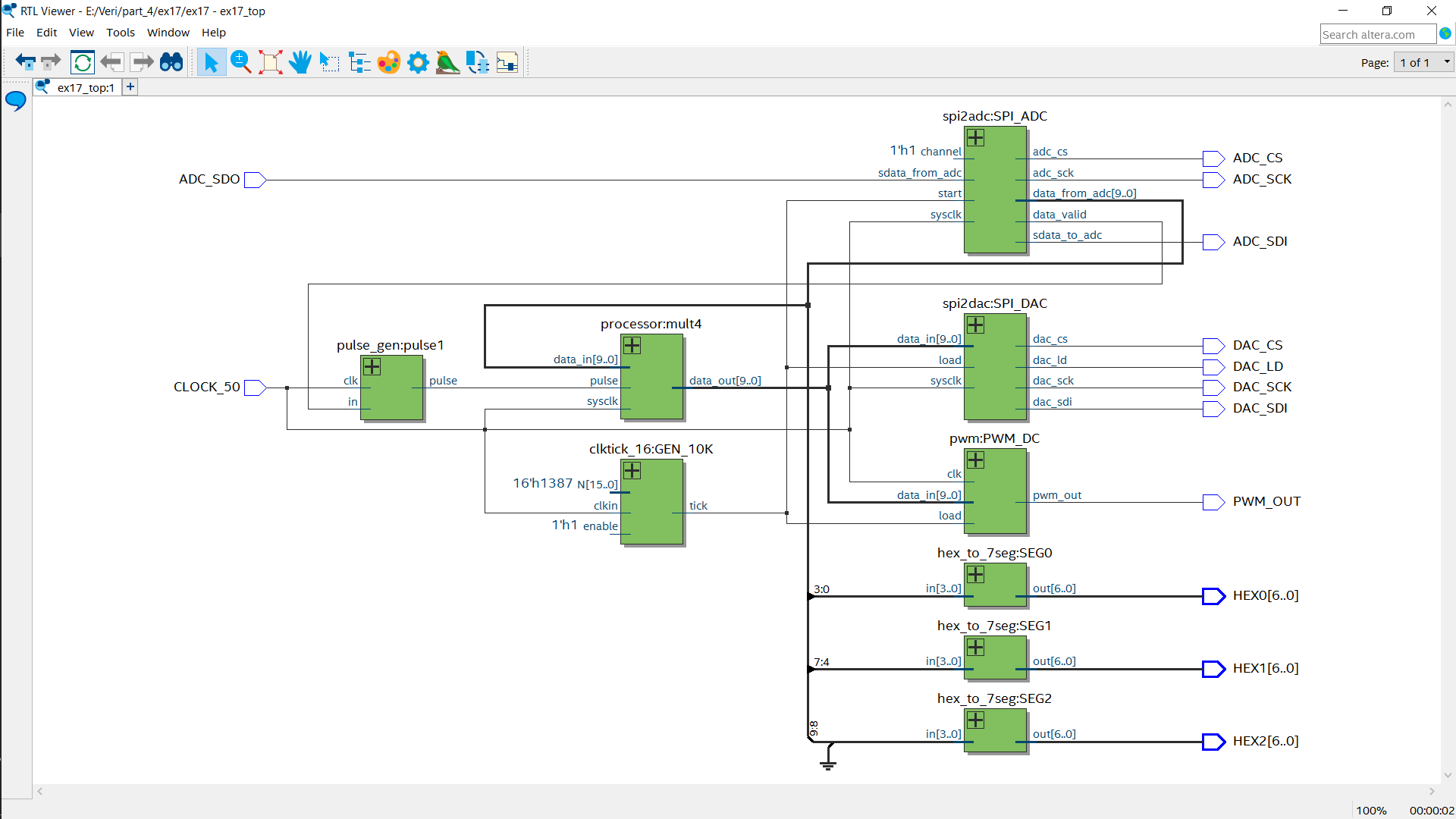
Verilog Experiment - Part 4

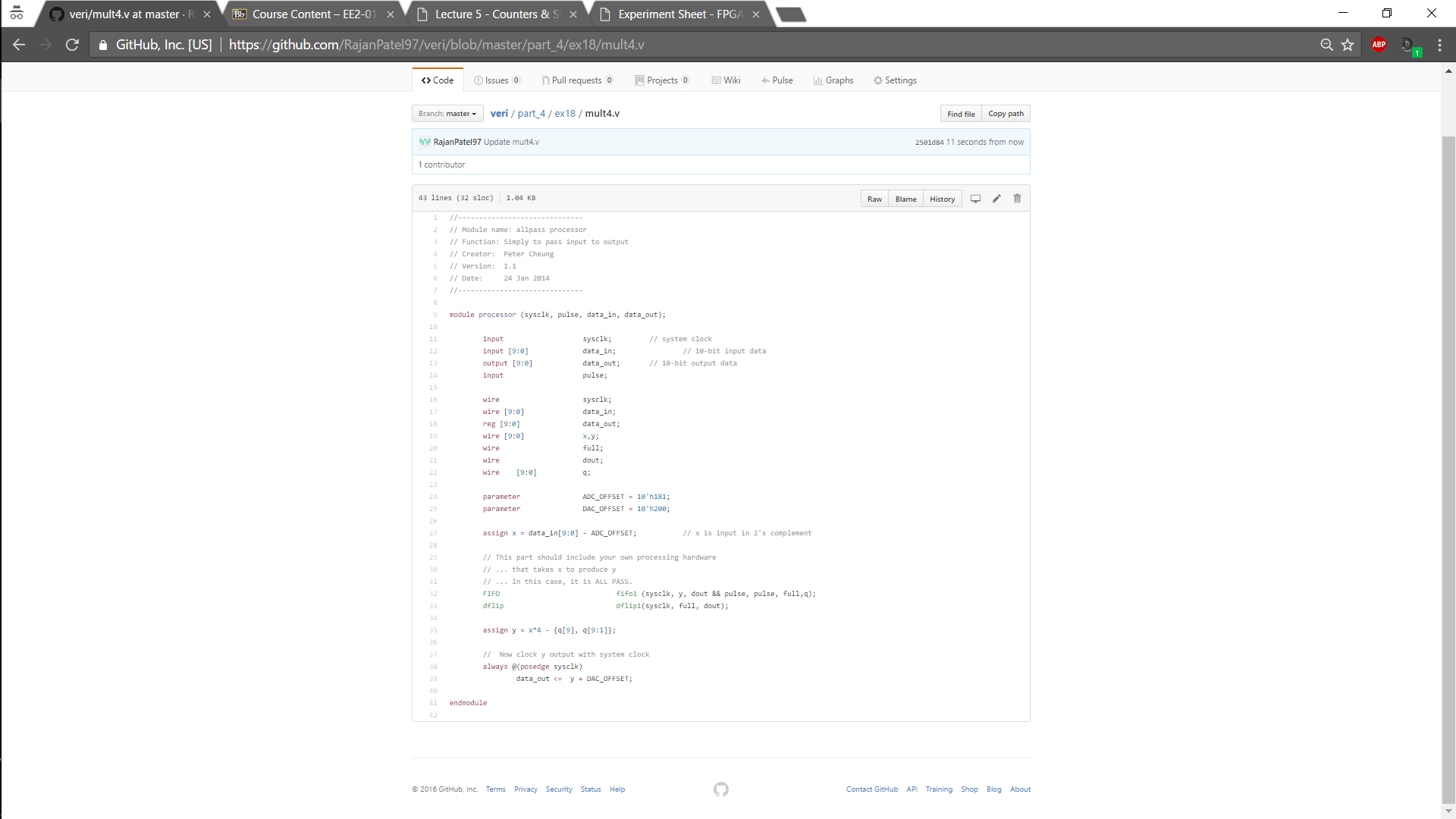
Experiment 16



Experiment 17





Experiment 18

