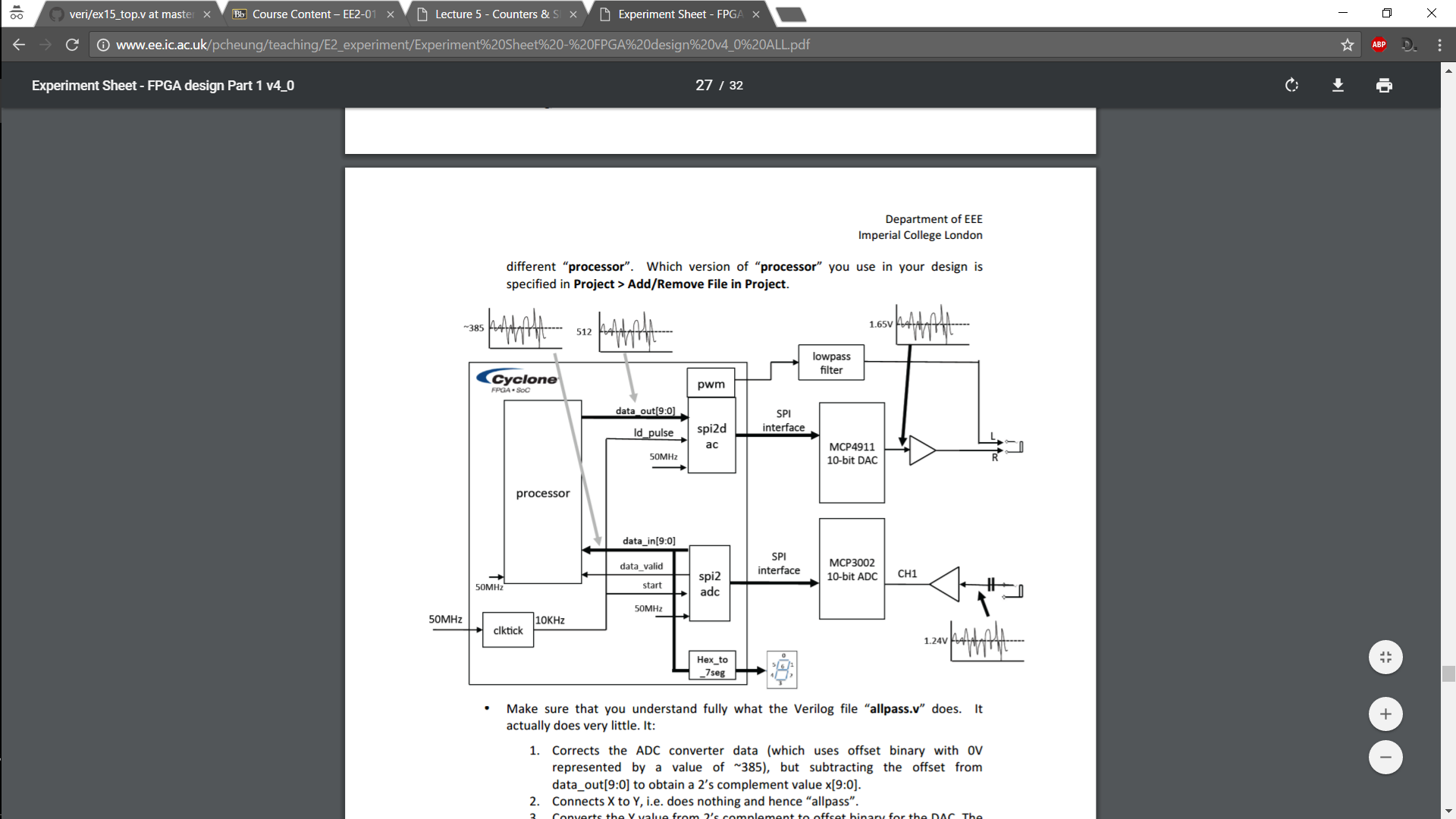
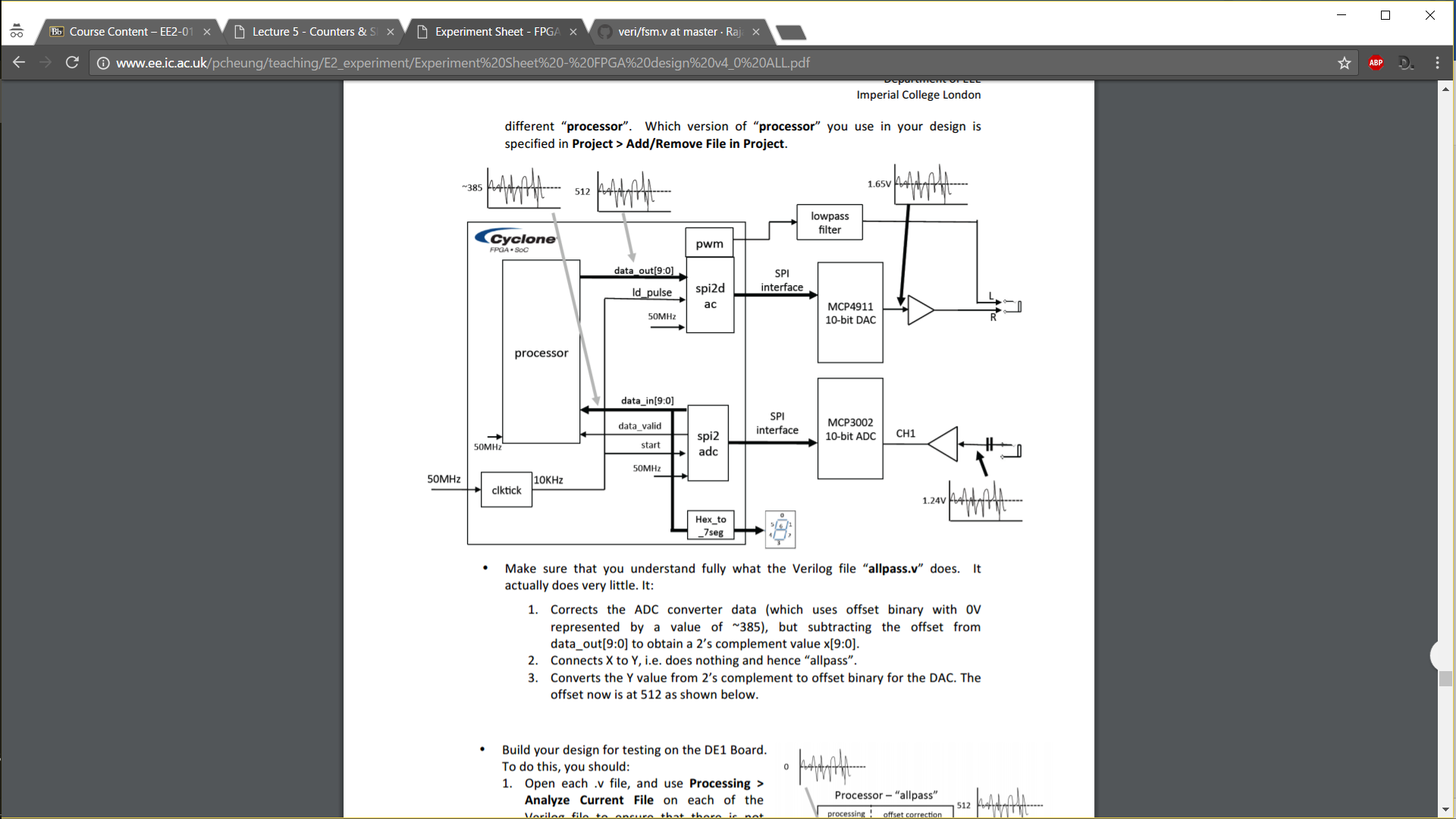
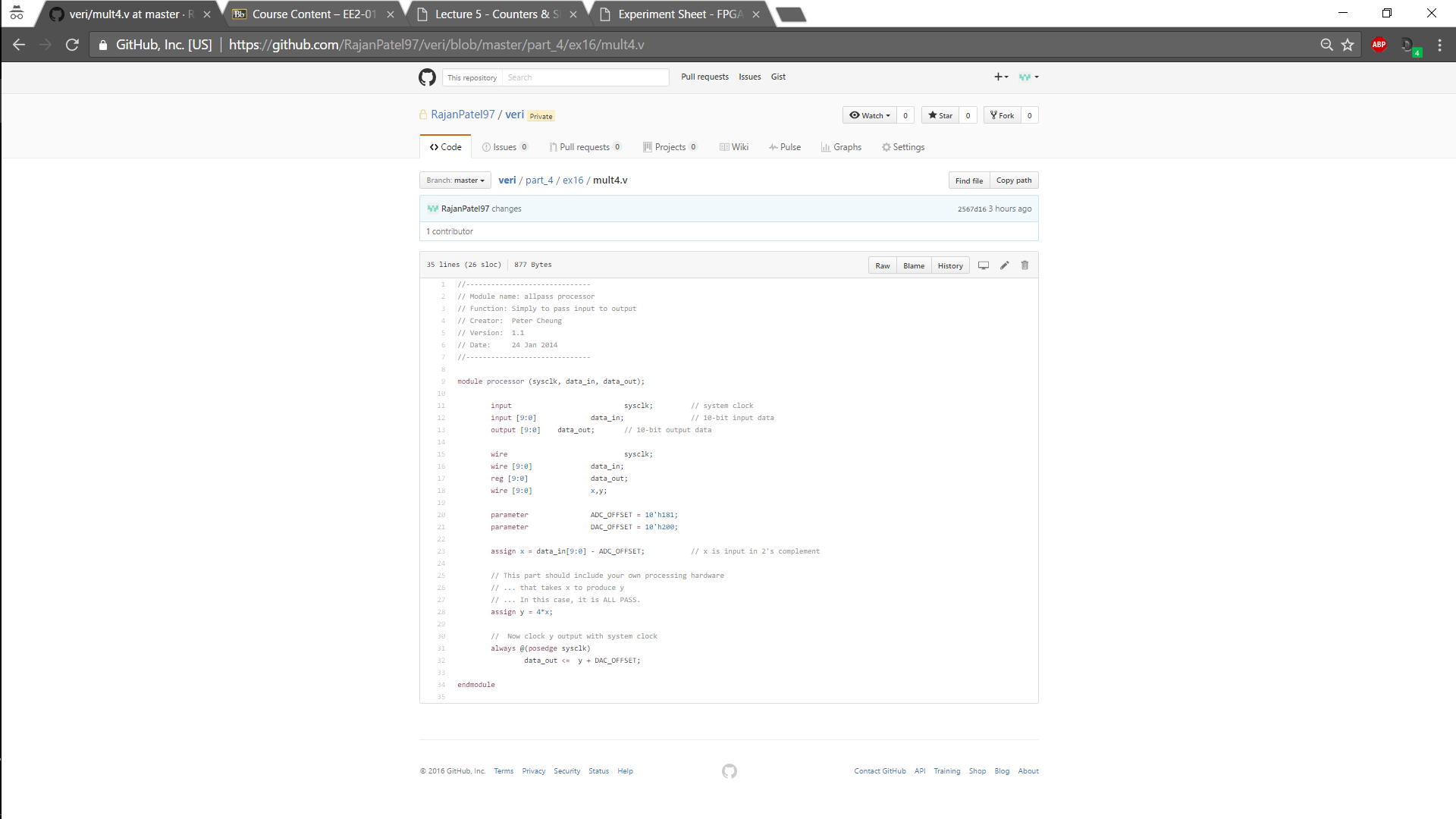
Verilog Experiment - Part 4

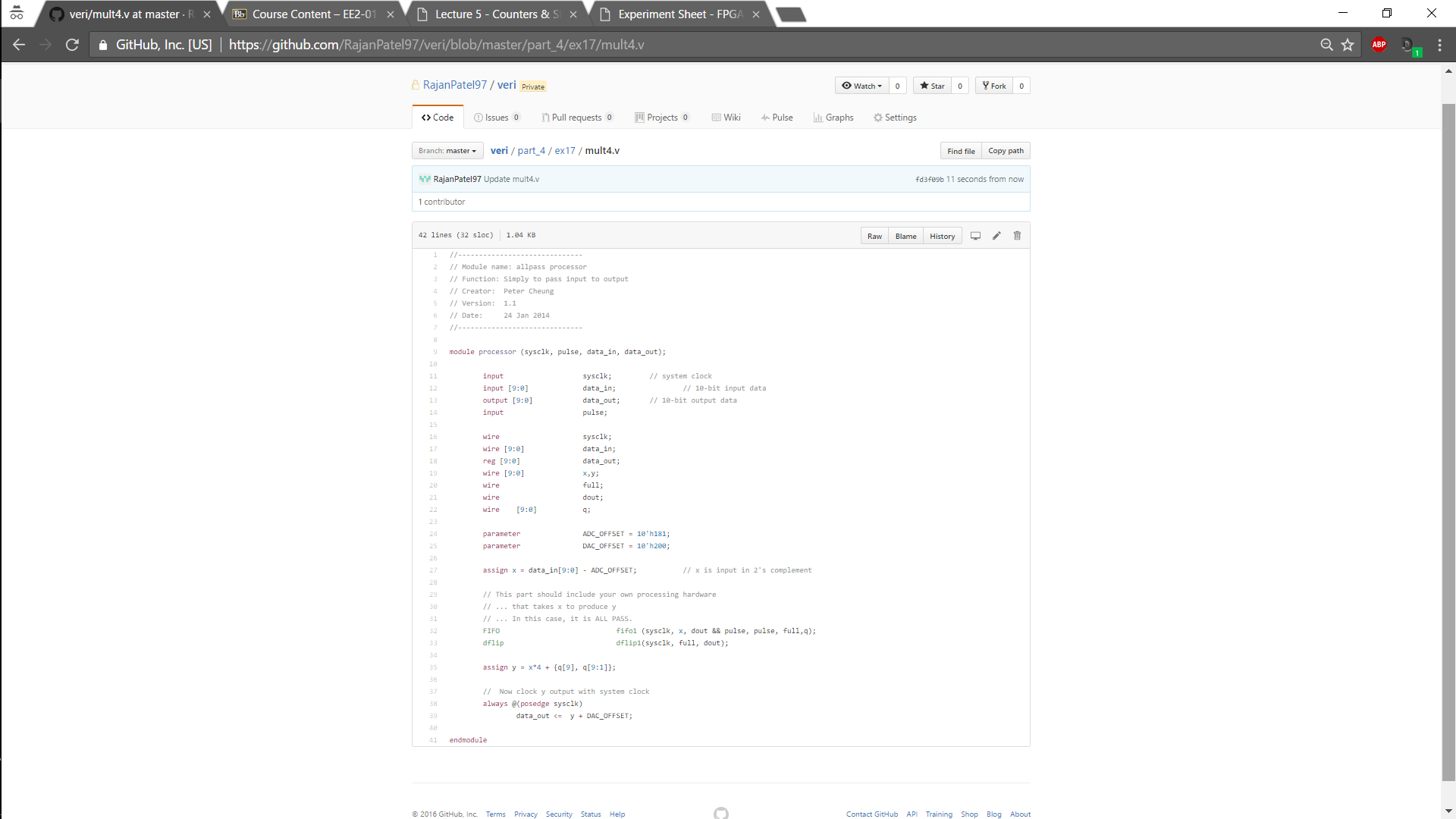
Experiment 16



The allpass processor module works in the following way:

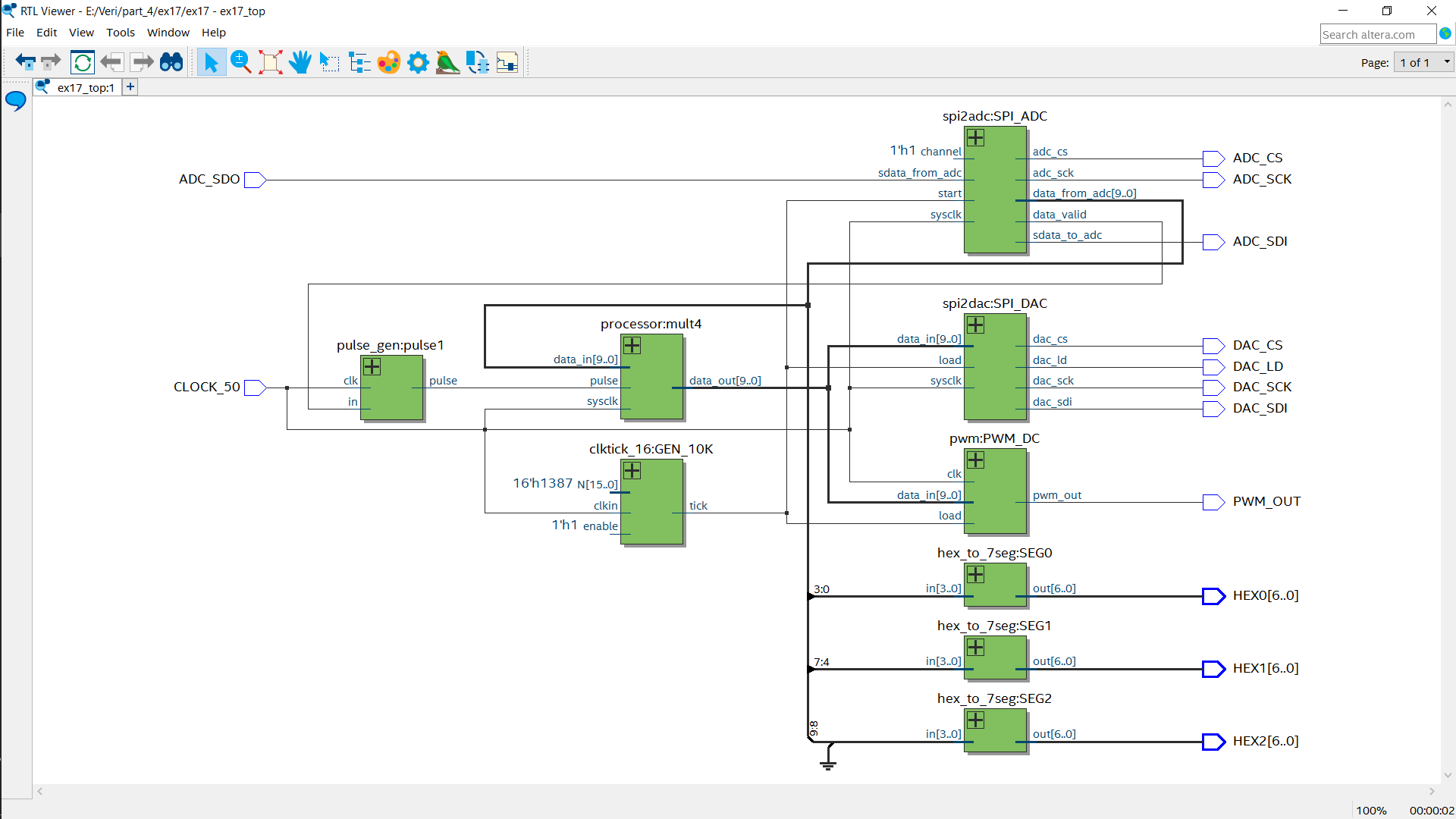


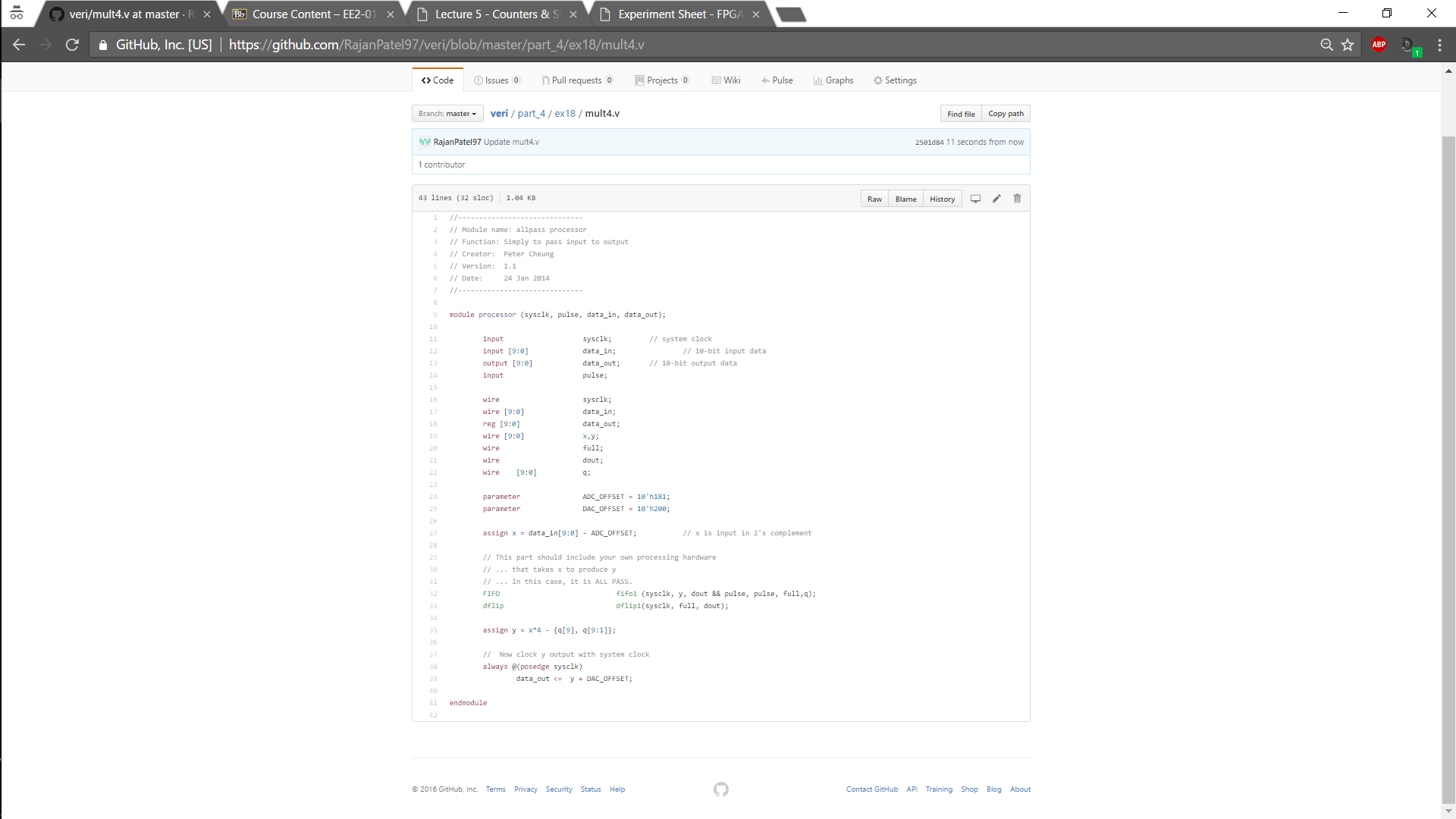
My multiplication processor works in the same way but multiplies the 2’s compliment input by 4 in order to get a louder output. The spi2adc uses dot notation so that signal names inside the module connect to outside the module in any order which is much safer. Outside the processor the code is the same, so it is very flexible and reusable.

Experiment 17

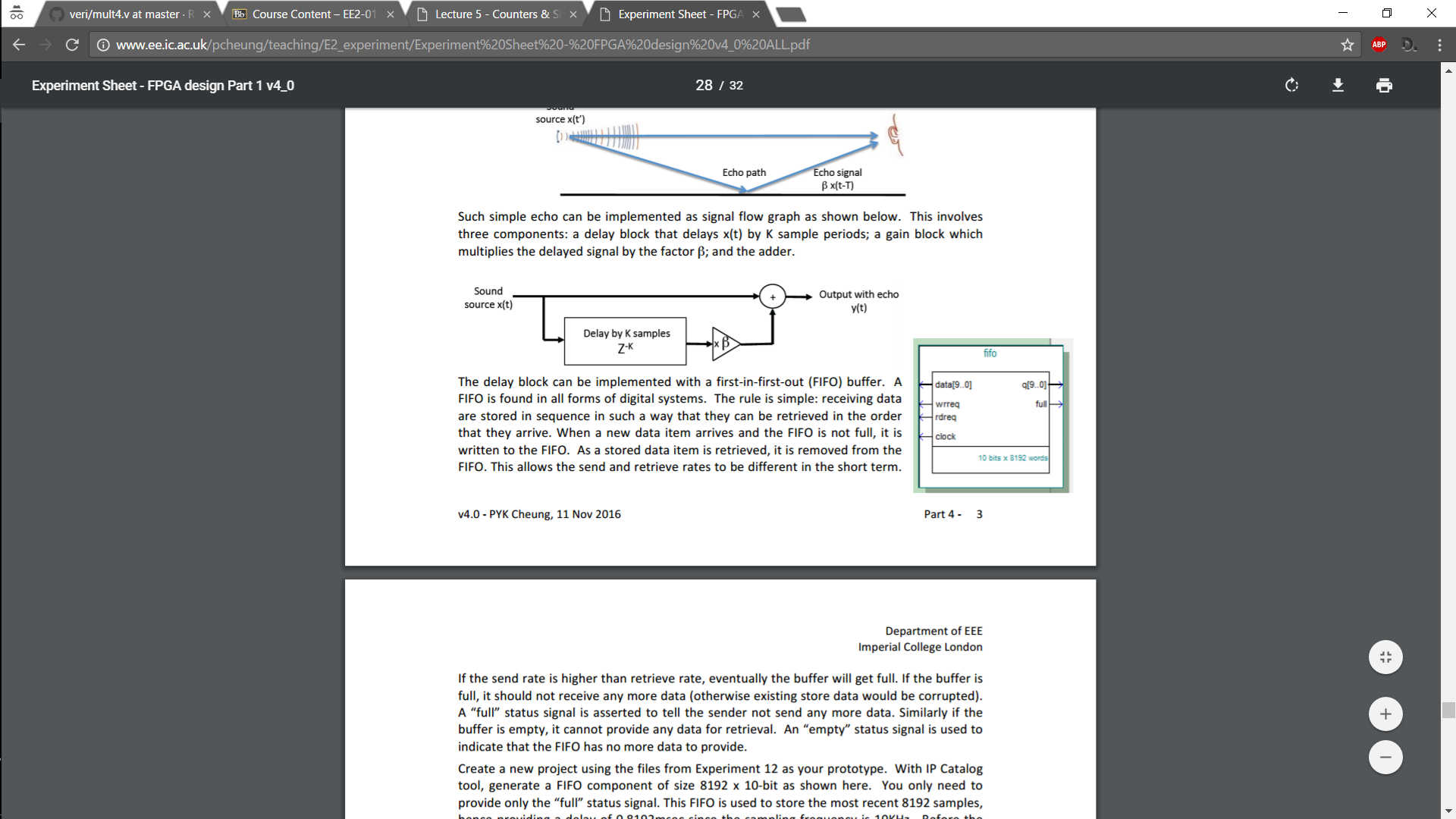
This new processor produces a single echo on an audio input using an 8192 x 10 bit FIFO. The FIFO delays the output by 0.8192s until it is full and then sends a full signal, thus the writing of the samples thereafter become synchronous. The current input is added to the delayed input giving the echo effect. The echo is attenuated by 0.5 or 0.25 so that upon addition it does not saturate the signal. The sampling frequency is 10KHz.

The top- level stays the same, only the processor changes.



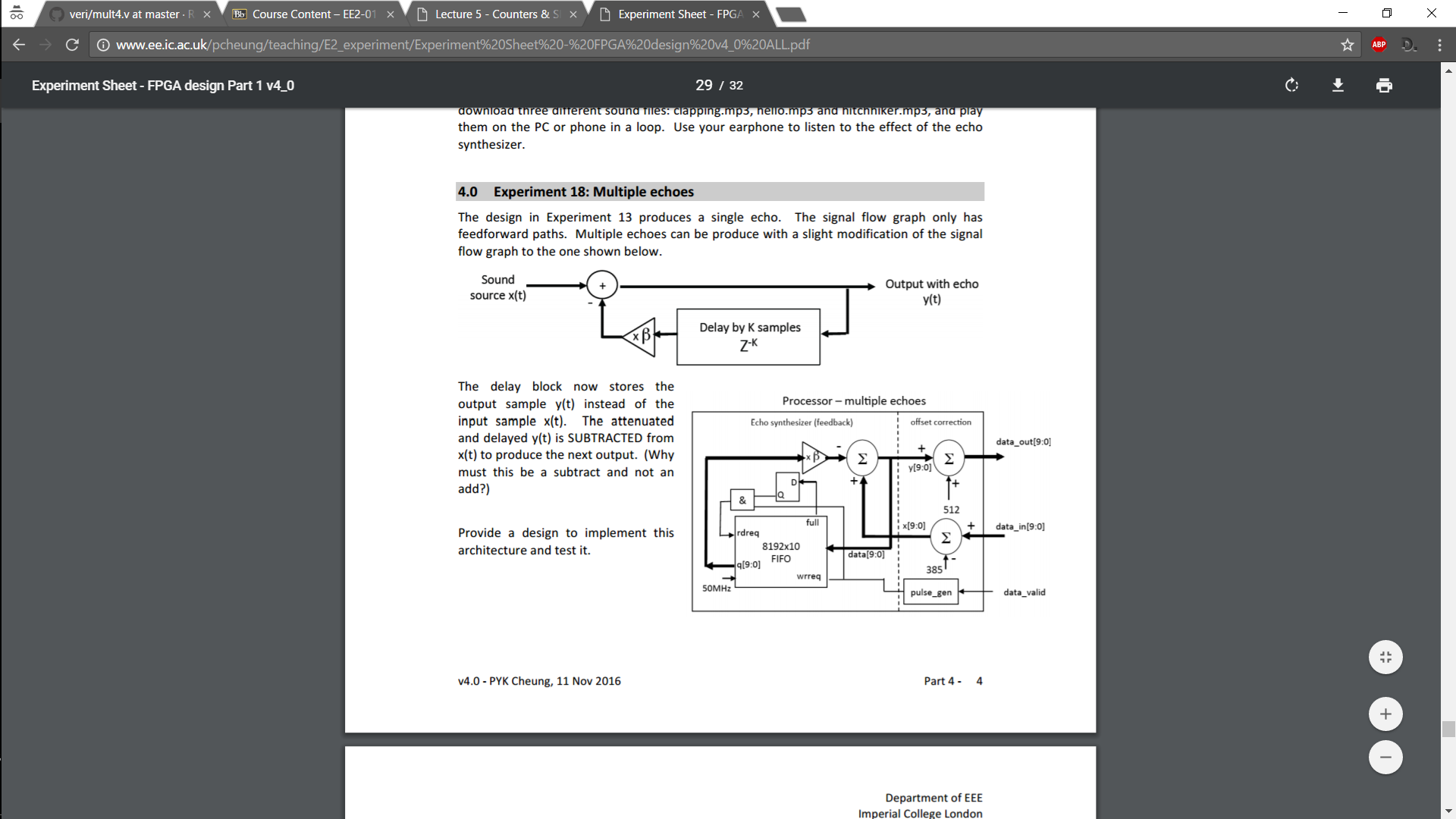
Experiment 18

This processor is very similar to the previous one, except that the delayed output is fed back in and subtracted from the current output giving multiple echoes. The difference is highlighted in the block diagrams below.

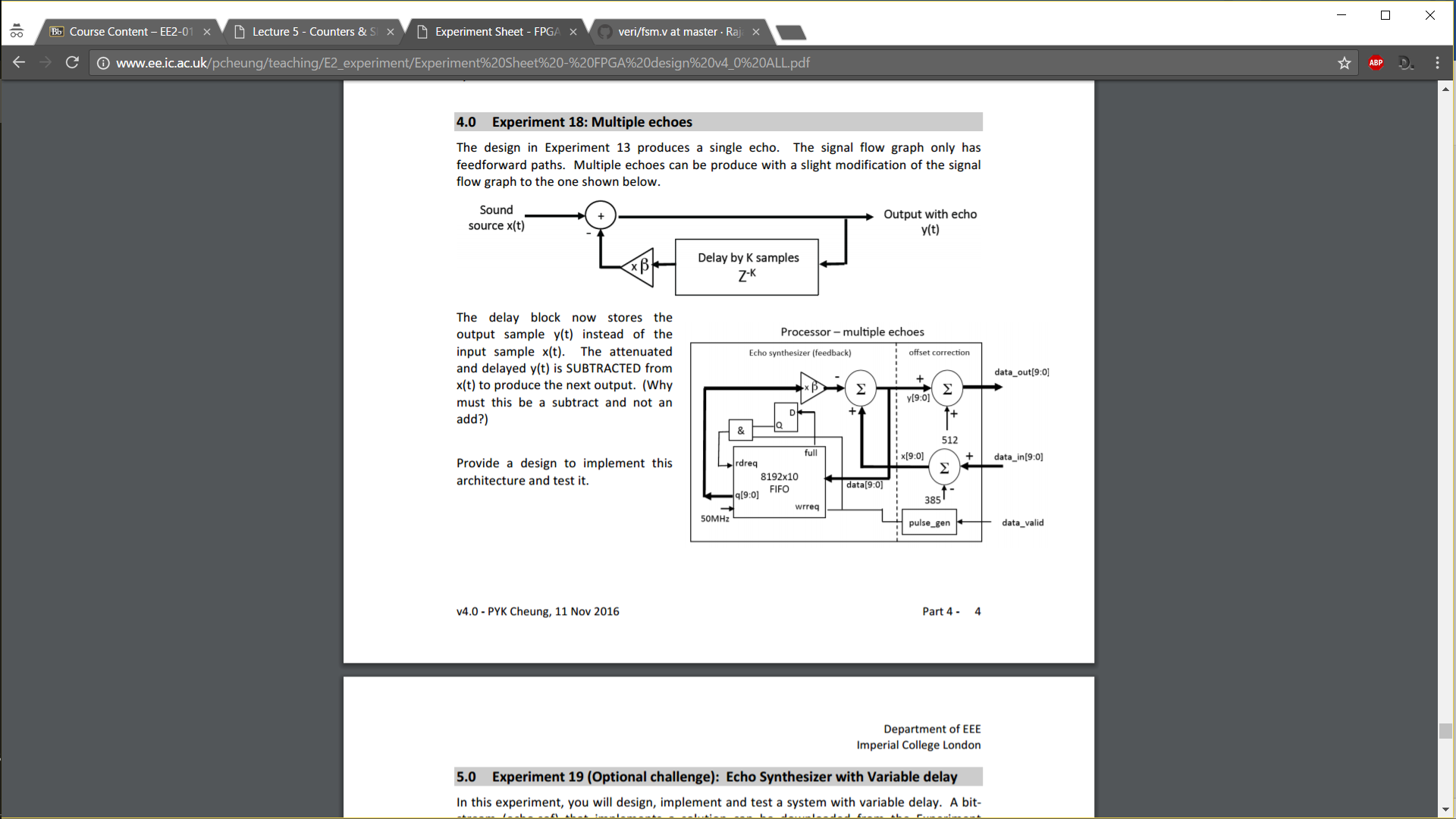


ONE ECHO

MULTIPLE ECHOES



Simplified Processor Block Diagram

One can see how this can be changed to obtain experiment 17 processor, as described above. I didn’t show RTL block diagram as too difficult to easily see difference between experiment 17 and 18.